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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/549,940

09/20/2005

Gunther Klage

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09/29/2006

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EXAMINER

LE, DINH THANH

ART UNIT

PAPER NUMBER

2816

DATE MAILED: 09/29/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/549,940

Applicant(s)

KLAGE, GUNTHER

Examiner

DINH T. LE

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☐ Responsive to communication(s) filed on ____.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-14 is/are pending in the application.
- 4a) Of the above claim(s) ____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) ____ is/are allowed.
- 6) ☒ Claim(s) 1-14 is/are rejected.
- 7) ☐ Claim(s) ____ is/are objected to.
- 8) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on ____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. ____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date 9/20/06.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. ____.
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: ____.

DETAILED ACTION

Specification

The specification has been checked to the extent necessary to determine the presence of all possible minor errors. However, the applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections

Claim Rejections - 35 USC § 112

Claims 3-8 and 13-14 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Correction or clarification is required.

In claim 3, the recitation “the low frequency range” on line 2 lacks clear antecedent basis. It is unclear what the range is.

In claim 4, it is unclear where the common reference frequency comes from, and how this frequency can be “synchronized” with the accumulator, the adder and the converter.

In claim 5, the recitation “the noise signal” lacks clear antecedent basis. It is unclear where the “noise signal” and “common reference clock pulse” on line 4 and “frequency divider” on line 4 come from and how the signal can be “bandpassed-filtered since no means for performing this function is recited in this claims.

In claim 13, it is unclear where the frequency divider and a switching element come from. The description of the present invention is incomplete because the claimed divider and

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switching element are not connected to anything. Thus, they may not perform the recited function.

In claim 14, the recitation "or" on line 3 is indefinite because it does not positively recite the claimed invention.

The remaining claims are dependent from the above rejected claims and therefore also considered indefinite.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-4 are rejected under 35 USC 102 (b) as being anticipated by Kerr et al (US 4,901,265).

As the best construed, Kerr et al discloses in Figure 1 a circuit comprising:

- an accumulator (12);
- a memory unit (16);
- an adder (26) coupled to a noise generator (24);
- a digital to analog inverter (18) and
- a filter (20).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior

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art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1-4 and 10 are rejected under 35Usc 103 (a) as being unpatentable over Reinhardt et al (US 5,014,231) in view of Kerr et al (US 4,901,265) in view of Semenov et al (US 4,653,001).

Reinhardt et al discloses in Figure 6 a synthesizer circuit comprising:

- an accumulator (14);
- a memory unit (12);
- an adder (18) coupled to a noise generator (16); and
- a digital to analog inverter (20).

However, Reinhardt et al does not disclose the low pass filter as recited in claim 1 and the high pass filter as recited in claim 10.

Kerr et al discloses in Figure 1 a filter circuit comprising a low pass filter(20) for removing noise components generated during conversion process, see lines 40-55, column 5.

Semenov et al suggests in Figure 1 a circuit comprising a high pass filter 8) placed after a low pass filter (7) for removing DC component, see lines 10-20, column 5.

It would have been obvious to a person having skill in the art at the time the invention was made to employ the low pass filter as suggested by Kerr et al and the high pass filter as suggested by Semoenov et al in the circuit of Reinhardt et al for the purpose of removing noise components generated during conversion process and for a DC component

Claims 10 are rejected under 35 USC 103 (a) as being unpatentable over Kerr et al (US

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4,901,265) in view of Semenov et al (US 4,653,001).

Kerr et al discloses in Figure 1 a circuit comprising all of the limitations of the claimed invention as stated above but does not disclose the high pass filter.

Nevertheless, Semenov et al suggests in Figure 1 a circuit comprising a high pass filter 8) placed after a low pass filter (7) for removing DC component, see lines 10-20, column 5.

It would have been obvious to a person having skill in the art at the time the invention was made to employ the high pass filter as suggested by Semenov et al in the circuit of Kerr et al for the purpose of removing DC component.

Claims 1-4, 10 and 11-12 are rejected under 35 USC 103 (as) as being unpatentable over Itoh et al (US 5,184,093) in view of Reinhard et al (US 5,014,231) and further in view of Semenov et al (US 4,653,001).

Itoh et al discloses in Figures 5-6 and 10 a synthesizer comprising:

- an accumulator (11); a memory (13); a converter (14); and a filter (15);
- a synthesizer comprising:
 - a phase detector (3); a mixer (16); a filter (4); a VCO (5); an oscillator (17) and a divider (7).
- However, Itoh et al does not disclose the noise generator and an adder being placed after the memory (13) as recited in claim 1, a high pass filter being placed after the low pass filter (15) as recited in claim 10 and the oscillator (17) is a PLL circuit as recited in claim 14.
- Reinhardt et al suggests in Figure 6 a noise generator (16) and an adder (18) for reducing the special spurious sidebands and phase noise, see lines 55-67, column 11.

Nevertheless, Semenov et al suggests in Figure 1 a circuit comprising a high pass filter 8) placed after a low pass filter (7) for removing DC component, see lines 10-20, column 5.

It would have been obvious to a person having skill in the art at the time the invention was made to employ the noise generator and the adder as suggested by Reinhardt et al and the high pass filter as suggested by Semenov et al for the purpose of reducing the special spurious sidebands and the phase noise, and for removing the DC component. Noted that, as well known in the art the PLL circuit is a means for generating a variable frequency signal compared to the oscillator (17). Thus, employing the PLL is considered to be a matter of a design expedient for an engineer depending upon a particular application. It would have been obvious to a person having skill in the art at the time the invention was made to employ the PLL in the circuit of Itoh et al for the purpose of providing a reference signal having variable frequency.

With regard to claim 13, since the divider (7) is used in the circuit of Itoh et al to step down the frequency from the mixer in order to match with the frequency of the signal f_d from the DDS (1). If the frequencies is matched, the divider (7) would not be needed. Thus, placing a bypass switch to switch out the divider is considered to be a matter of a design expedient depending upon the particular application in which the circuit of Reinhardt et al is to be used and that would have been obvious at the time of the invention

Allowable Subject Matter

Claims 5-9 are allowed because the prior art of record fails to show the divider connected to a common reference clock pulse as combined in claim 5.

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Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to DINH T. LE whose telephone number is (571) 272-1745. The examiner can normally be reached on Monday-Friday (8AM-7PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, TIMOTHY CALLAHAN can be reached at (571) 272-1740.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

9/27/06

DINH T. LE
PRIMARY EXAMINER
